Search Results

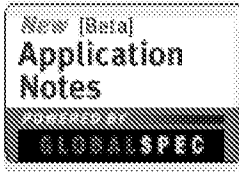BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPORT

Results for "(((integrated and circuit and des and register)<in>metadata)) <and> (pyr >= 1950 <..."
Your search matched 4 of 1820465 documents.
A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

e-mail   printer f

New [Beta]
Application
Notes
GLOBALSPEC

- Search Options

View Session History

New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(((integrated and circuit and des and register)<in>metadata)) <and> (pyr >= 1950 <ar   Search >

☐ Check to search only within this results set

Display Format: ● Citation   ○ Citation & Abstract

IEEE/IET   Books   Educational Courses   Application Notes [Be

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and standards.

view selected items   Select All Deselect All

☐   1. Design of a low-power 32 K CMOS programmable delay-line memory
          Dejhan, K.; Demassieux, N.; Colavin, O.; Galisson, A.; Artieri, A.; Jutand, F.;
          Solid-State Circuits, IEEE Journal of
          Volume 25, Issue 1, Feb. 1990 Page(s):234 - 238
          Digital Object Identifier 10.1109/4.50309

          AbstractPlus | Full Text: PDF(508 KB)   IEEE JNL
          Rights and Permissions

☐   2. A new high-performance programmable delay line IC
          Dejhan, K.; Jutand, F.; Demassieux, N.; Colavin, O.; Galisson, A.; Artieri, A.;
          Consumer Electronics, IEEE Transactions on
          Volume 35, Issue 4, Nov. 1989 Page(s):893 - 900
          Digital Object Identifier 10.1109/30.106914

          AbstractPlus | Full Text: PDF(528 KB)   IEEE JNL
          Rights and Permissions

☐   3. SEU testing of a novel hardened register implemented using standard CMOS technology
          Monnier, T.; Roche, F.M.; Cosculluela, J.; Velazco, R.;
          Nuclear Science, IEEE Transactions on
          Volume 46, Issue 6, Dec. 1999 Page(s):1440 - 1444
          Digital Object Identifier 10.1109/23.819105

          AbstractPlus | Full Text: PDF(224 KB)   IEEE JNL
          Rights and Permissions

☐   4. A ring architecture strategy for BIST test pattern generation
          Fagot, C.; Gascuel, O.; Girard, P.; Landrault, C.;
          Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian
          2-4 Dec. 1998 Page(s):418 - 423
          Digital Object Identifier 10.1109/ATS.1998.741650

          AbstractPlus | Full Text: PDF(1156 KB)   IEEE CNF
          Rights and Permissions